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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/204,479	12/03/1998	MARC TREMBLAY	SP-3289US	5561

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EXAMINER

ENG, DAVID Y

ART UNIT	PAPER NUMBER
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2155

DATE MAILED: 11/20/2001

14

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/204,479

Applicant(s)

TREMBLAY ET AL.

Examiner

DAVID Y. ENG

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 8/27/2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-17 and 19-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-17 and 19-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Pri ority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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Claims 1, 3-17 and 19-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In review of the amendment filed on August 27, 2001, portion of the rejection under this section set forth in the previous Office action is withdrawn. The remaining issues are rewritten as follow.

7 In claim 7, it is not clear how the recitation in lines 5-8 is related to control transfer. The address represented by the word "label" per se in the call instruction is sufficient to cause a control transfer. Functions of the alias register and the alias link pointer Ip have not been recited.

19 With respect to claim 19, it is not clear what is meant by "the register file generating two pointers". Note that a register file is for storing or outputting operands in response to register specifiers. A register file does not generate pointers.

Further with respect to claims 1, 3-17 and 19-22, there is nothing recited in the claims to execute instructions in a manner as recited in dependent claims 3-16 as follow:


1, 3, 21-22 1. A decoder is commonly for decoding opcodes or for generating control signals in response to opcodes and not for deriving anything as recited in the claims. It appears that a decoder is unable to derive a specifier by adding two numerical numbers as recited. Only ALU or incrementer can do that. See claims 1, 3 and 21-22 for examples.

4 2. Claim 4 recites that registers are associated to functional units. If that is the case, the registers in the register file do not require register specifiers for accessing. The claim is vague and

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indefinite in that it is not clear how exactly the registers are addressed, by association or by addresses.

3. In claim 6, it is not clear what register rs2 and rd in instruction bitext are for.
4. In claim 9, a space is missing between two words.
5. In claim 17, function of the decoder is not clear. This can be corrected by inserting "pointing" after the two words "pointer".
6. In claim 20, the term "defining" in "defining a register specifier" is vague and indefinite. It is not clear what it means. Does it mean outputting, generating, retrieving, reading, writing, inserting, pointing, describing or copying, etc.?

 Applicants are requested to identify the portion of the specification which discloses how exactly Applicants' decoder implicitly derives a register specifier based on an explicitly-specified register specifier.

In response to the section 112, 2nd paragraph rejection, Applicants blanketly said that the claims are broad but not vague and indefinite. No explanation was provided to support why the defects are broad and not vague and indefinite. No attempt was made to correct the defects.

Applicants further state with respect to claim 19 that the meaning of the claims is clear in light of the specification. No portion of the specification is identified by Applicants.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

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Claims 1, 3, 5-17 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oliver (3,931,615) in view of Gebhardt (3,833,904).

With respect to claims 1 and 20-22, see at least Figure 1 and the corresponding description in Oliver. Oliver teaches a processor comprising:

a register file (item 12, col. 3 line 66),

a functional unit (ALU 17), and

a decoder (item 11, see col. 3 line 58).

Oliver further teaches in lines 57 et seq. of column 4 that a second source operand (rs1+1 in the claims) is derived implicitly without explicit identification in the instruction (no rs1+1 specified in the instruction operand fields). In Oliver, the second operand is not required to be explicitly specified in the operand field of an instruction. Instead, it is implicitly derived as claimed by applicants. In Oliver, it appears that the second operand is implicitly derived by association (selection circuit) and not derived from the explicitly specified specifier by incrementing. However, Gebhardt teaches a processor having a plurality of functional units (col. 36 line 34) operating on operands. The second operand can be derived by incrementing the address of the first operand (lines 46 et seq. of column 36).

With respect to claims 3, 5-17 and 19, Gebhardt also teaches floating point (lines 35 et seq. of col. 221), double precision operation (lines 53 et seq. of col. 182).

From the combined teaching of both Oliver and Gebhardt, it would have been obvious to a person of ordinary skill in the art, when having both references before him, to implicitly specify a

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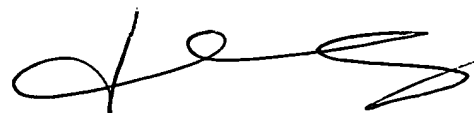
second operand as taught by Oliver by incrementing the address of the first operand as taught by Gebhardt in a double precision floating point processor of Gebhardt such that operand address space in an instruction can be shorter to improve memory space. Note that double precision floating point operand requires more address bits. It is well known to use implicit operand address to improve memory address space by shortening the operand fields in an instruction as taught by Oliver.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oliver (3,931,615) and Gebhardt (3,833,904) further in view of Chamandi (6,311,261).

Oliver and Gebhardt teach claim limitations set forth above. Neither Oliver nor Gebhardt state that their processor is a VLIW one. VLIW processor is well known in the art as disclosed by Chandani (lines 21 et seq. of col. 37). It would have been obvious to a person of ordinary skill in the art to use a VLIW processor in either Oliver or Gebhardt so as to improve processing power.

The Oguchi (6,249,167) and the Thusoo (5,790, 826) are cited for the teaching of implicitly deriving an operand address. See lines 38 et seq of column 4 in Thusoo and lines 30 et seq of column 15 in Oguchi.

Applicant's arguments with respect to claims 1 and 20 have been considered but are moot in view of the new ground(s) of rejection.



DAVID Y. ENG
PRIMARY EXAMINER